AMENDMENTS TO THE SPECIFICATION

Please replace the first full paragraph on page 11 with the following amended paragraph:

Fig. 8 is a diagram showing an example of the level shift core circuit 1 used for the level shift circuit depicted in Fig. 7. As shown in Fig. 8, the level shift core circuit 1 according to the present invention comprises a plurality of PMOSs ~~110~~, in which the second power supply (VDDH) is connected to the source of each PMOS, the two types of the level shift output signals OUTHB and OUTH are connected to the drains of the PMOSs, respectively, and the drain of each PMOS is cross-coupled with the gate of another PMOS. The level shift core circuit 1 further comprises: an NMOS ~~103~~ whose drain is connected to OUTHB, whose gate is connected to INL and whose source is connected to the ground voltage GND; and an NMOS ~~104~~ whose drain is connected to OUTH, whose gate is connected to INLB and whose source is connected to the ground voltage GND. While Fig. 8 shows two PMOSs and two NMOSs, there may be a plurality of cross circuits each including two PMOSs. In other words, the level shift core circuit may comprise, for example, the circuits as shown in Fig. 8 in plural numbers, which are connected to one another in parallel.

Please replace the third full paragraph on page 11 with the following amended paragraph:

The control circuit 2 exemplified in Fig. 9 comprises: a first NAND circuit ~~1021~~ fed from the second power supply (VDDH), which receives INL and OUTHB and outputs C0; a second NAND circuit ~~1022~~ fed from the second power supply (VDDH), which receives INLB and OUTH and outputs C1; a first inverter ~~1023~~ fed from the second power supply (VDDH), which

receives the output C0 of the first NAND circuit ~~1021~~ and outputs C3; and a second inverter ~~1024~~ fed from the second power supply (VDDH), which receives the output C1 of the second NAND circuit ~~1022~~ and outputs C2.

Please replace the third full paragraph on page 12 with the following amended paragraph:

Fig. 11 is a diagram showing an example of the NAND circuit ~~1021 or 1022~~ depicted in Fig. 9. Referring to Fig. 11, level shift input (INL or INLB) is connected to an NMOS 1 near the output terminal. With this construction, the gate delay can be reduced as compared to when the level shift input is connected to an NMOS 2 far from the output terminal. On the other hand, since the level shift input is at the first power supply level, in cases where the potential difference with the second power supply increases, where the threshold voltage (Vt) of the NMOS increases or, in particular, where the influence of an increase in the threshold voltage of the NMOS grows due to the substrate bias effect, the delay may develop if the level shift input (INL or INLB) is connected to the NMOS close to the output terminal. On such an occasion, the level shift input is connected to the NMOS 2 with little substrate bias effect far from the output terminal, and OUTH or OUTHB is input to the NMOS far from the output terminal. Thereby, the delay can be reduced.

Please replace the second full paragraph on page 16 with the following amended paragraph:

In the level shift circuit according to the first embodiment of the present invention, the level shift core circuit 1 may be implemented with different circuitry than that described previously for the first embodiment in connection with Fig. 8. For example, as shown in Fig. 16,

a PMOS switch may be provided to the respective drain sides of the PMOS cross-coupled pair. The level shift circuit operates in the same manner as in the first embodiment set forth hereinbefore, and the description will not be repeated here. According to the modified example of the first embodiment, with the level shift core circuit 1 of Fig. 16, the bond of the PMOS cross-coupled pair can be further weakened when the first power supply voltage (VDDL) falls as compared with the level shift core circuit of Fig. 8. More specifically, as can be seen in Fig. 16, the level shift core circuit comprises a PMOS cross-coupled pair (a pair of PMOSs), a pair of PMOS switches (another pair of PMOSs), and a pair of NMOSs. The second power supply (VDDH) is connected to the source of each PMOS ~~110~~ of the cross-coupled pair (a pair of PMOSs). The two types of the level shift output signals OUTHB and OUTH are connected to the gates of the PMOS cross-coupled pair, respectively, and the drains of the PMOS switches, respectively. The source of each PMOS switch is connected to the drain of one of the PMOSs. The NMOSs includes: an NMOS ~~103~~ whose drain is connected to OUTHB, whose gate is connected to INL and whose source is connected to the ground voltage GND; and an NMOS ~~104~~ whose drain is connected to OUTH, whose gate is connected to INLB and whose source is connected to the ground voltage GND. As just described, a couple of the PMOS switches composed of PMOSs ~~111 and 112~~ are provided between the PMOS cross-coupled pair and the NMOSs. Thus, the strength of the cross bond between the PMOSs forming the PMOS cross-couple can be reduced, and transition between high and low can be accelerated.

Please replace the second full paragraph on page 17 with the following amended paragraph:

As a substitute for the level shift core circuit 1 of Fig. 8 or 16, a circuit as shown in Fig. 17 may be employed~~. The level shift core circuit 1, in which the level shift output is connected to the first power supply (VDDL), controlled by level shift input signals may be applied to the level shift circuit of the first embodiment. The level shift circuit provided with such level shift core circuit 1 can help the NMOS 103 change to high and the NMOS 104 change to low.~~ The level shift core circuit 1 includes two pull-up NMOSs each having a source connected to the level shift output, a gate connected to the level shift input, and a drain connected to the first power supply (VDDL), thus supporting the transition of the outputs to high. Thereby, a level shift can be performed at a higher speed. In addition, the margin of level shift operation can be ensured when the potential difference between the first and second power supplies increases.

Please replace the second full paragraph on page 28 with the following amended paragraph:

More specifically, in the case where INL is low, INLB is high, OUTH is low, and OUTHB is high, when the INL signal output from the first logic circuit has changed to high (INLB has changed to low)~~, the control circuit 2 outputs the C4 signal and the like in response to the input of the INL signal. The low C4 output is input to the level shift core circuit 1 and turns on the PMOS therein. Thus, the PMOS pulls up OUTHB. Consequently,~~ the control circuit 2 outputs high C4 to turn off the PMOS switch connected to OUTHB in the level shift core circuit 1, thereby inhibiting OUTHB from being pulled up. On the other hand, when OUTHB has been pulled down to low due to the operation of the level shift core circuit 1~~, the PMOS in the level shift core circuit which receives OUTHB through the gate turns on, and also the PMOS in the level shift core circuit which receives C5 through the gate turns on, each terminating the pull-up~~

~~operation of the other. At the same time, the control circuit 2 outputs low C3 so that the NMOS of the pull-up and/or pull-down circuit 3 turns off to terminate the pull-down operation. The control circuit 2 also outputs~~ the control circuit 2 low C4 to turn on the PMOS switch in the level shift core circuit. As a result, INL becomes high, INLB becomes low, OUTH becomes high, and OUTHB becomes low.

Please replace the first full paragraph on page 29 with the following amended paragraph:

Subsequently, when INLB output from the external first logic circuit 4 has changed to high (INL has changed to low), ~~the control circuit 2 outputs low C4 in response to the input of the signal. Accordingly, the PMOS connected to OUTHB in the level shift core circuit 1 turns on to pull up OUTHB. Further, the control circuit 2 outputs high C5 so that the NMOS connected to OUTH turns on in the level shift core circuit 1 to pull down OUTH. The~~the control circuit 2 outputs high C5 to turn off the PMOS switch connected to OUTH in the level shift core circuit 1, thereby inhibiting OUTH from being pulled up. On the other hand, when OUTH has been pulled down to low due to the operation of the level shift core circuit 1, the ~~control circuit 2 outputs high C4 so that the PMOS in the level shift core circuit 1 turns off to terminate the pull-up operation. The~~ control circuit 2 also outputs low C5 to turn off the NMOS in the level shift core circuit 1. As a result, INL becomes low, INLB becomes high, OUTH becomes low, and OUTHB becomes high. Incidentally, the description has been made of the case where the level shift core circuit 1 having NMOSs (transistors) and PMOSs (transistors) as described previously in connection with Fig. 33 is employed. In the case, however, the NMOSs are replaced by

PMOSs and/ or the PMOSs are replaced by NMOSs, the connections with the OUTH and

OUTHB signals are changed, and these changes are reflected in the above-described operation.